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AUTHOR(S):

Miura, M; Nakamura, S; Suda, J; Kimoto, T;
Matsunami, H

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Fabrication of SiC Lateral Super Junction Diodes With Multiple Stacking p- and n-Layers

Mineo Miura, Shun-ichi Nakamura, Jun Suda, Tsunenobu Kimoto, and Hiroyuki Matsunami, *Fellow, IEEE*

Abstract—Using epitaxial multiple p-n junction structures of 4H-SiC, lateral super junction diodes were fabricated for the first time. The breakdown voltage of the device was 400 V, which is more than 3× higher than the theoretical value calculated for a device with uniformly-doped drift layer (130 V), indicating the effective operation of super junction structure.

Index Terms—Power device, silicon carbide (SiC), super junction.

I. INTRODUCTION

THE requirements for power devices are high blocking voltage, low losses and high switching speed. Because of a tradeoff among them, many structures of devices have been developed for various applications. The semiconductor material mainly used for power devices is silicon (Si), but the extensive and intensive progress in Si processing technologies have brought the device performance close to the theoretical limitation expected from Si material properties. One way to make a breakthrough beyond the limitation may be the use of another material.

One of the most promising semiconductor materials for power devices is silicon carbide (SiC) [1], owing to its wide bandgap (2.2 to 3.4 eV), high breakdown field (around 3 MV/cm), and high thermal conductivity (4.9 W/cmK). Different from other wide bandgap materials, both n- and p-type conductivity of SiC can be easily controlled by both epitaxial growth and ion implantation. There have already been reported several SiC Schottky and p-i-n diodes [2] exceeding the limitation of Si.

For further improvement, a super junction (SJ) structure [3] has been proposed, which consists of highly-doped multiple thin p-n junctions. As opposed to ordinary device structures, the voltage is applied along, rather than across, the junctions. Lateral extension (perpendicular to the applied voltage) of the depletion region(s) in the SJ causes full depletion of the SJ at a small reverse bias, and further reverse voltages are supported by the fully depleted SJ with almost uniform distribution of electric field, regardless of doping concentration. Therefore, a high doping concentration can be utilized, compared with conventional structures with the same blocking voltage, yielding much

lower specific on-state resistance (R_{on}). In a simulation for Si [3], the R_{on} of SJ structure was predicted to be 100× lower than that of conventional one.

There have been a few reports on simulation of SiC SJ devices [4], [5], predicting 140× lower R_{on} of 4H-SiC SJ vertical devices than that of SJ devices made of Si [4], but no report on fabrication of SiC SJ devices has been presented. A lateral SJ structure is advantageous in device fabrication processes for SiC: a lateral SJ structure (or multiple thin p-n junctions) can be formed by epitaxial growth [6], [7], because dopant redistribution during epitaxial growth of SiC is negligible due to small diffusion coefficients in spite of high growth temperatures (normally 1500–1600 °C). For lateral SJ devices, the R_{on} shows a square dependence on the blocking voltage, as opposed to a linear dependence for vertical SJ devices [3]. Therefore, lateral SJ devices will have higher R_{on} than that of vertical ones. This weak point can, however, be compensated by increasing the number of p-n junction layers in the SJ structure to reduce the R_{on} . In this letter, simulation and fabrication of SiC lateral SJ diodes are presented.

II. NUMERICAL SIMULATION OF SiC SUPER JUNCTION

To simulate SiC SJ device structures, ISE-TCAD was used. As material properties of 4H-SiC, we assumed a bandgap of 3.26 eV, dielectric constant of 9.66 [8], mobilities of electrons and holes in [9], and impact ionization coefficients along the $\langle 0001 \rangle$ direction (though we need those in the $\{0001\}$ plane) in [10]. As the breakdown field in 4H-SiC shows strong anisotropy [11], the impact ionization coefficients should also have strong anisotropy (not reported yet). The actual breakdown voltage may be estimated by multiplying the ratio of the breakdown fields in the $\{0001\}$ plane and along the $\langle 0001 \rangle$ direction (approximately 0.75 [11]).

Different from conventional device structures, the blocking voltage of SJ devices does not depend on the doping concentration, but solely on the length of the SJ structure along which the voltage is applied. From the limitation of our lithography system, we selected the length of SJ to be 10 μm . The corresponding blocking voltage was calculated to be 1.3 kV, with the anisotropy of breakdown field taken into account. The R_{on} decreases with increasing doping concentration in the SJ, but an imbalance of doping concentration in the SJ significantly reduces the blocking voltage [3], [4]. From the uniformity and controllability of doping during our epitaxial growth, we selected the doping concentration of $4 \times 10^{17} \text{ cm}^{-3}$. The corresponding optimal thickness of the SJ layers was calculated to be 0.4 μm . An important simulation result is that the thickness

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The authors are with the Department of Electronic Science and Engineering, Kyoto University, Kyoto 606-8501 Japan.

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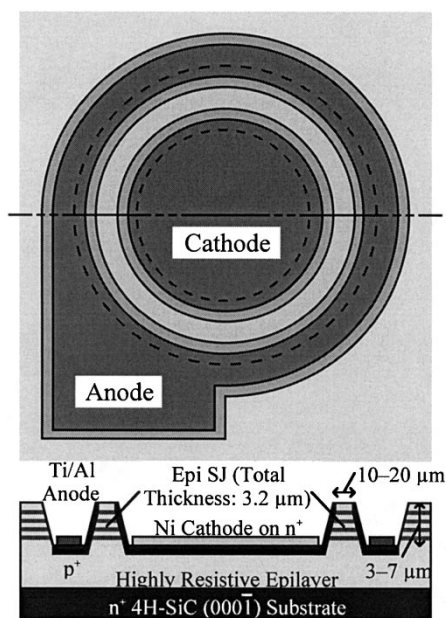


Fig. 1. Schematic structure of fabricated devices. The device active area is indicated by dashed circles.

of the outermost layers in a finite SJ should be halved; otherwise incomplete depletion in the outermost layers distorts the electric field distribution and reduces the breakdown voltage less than half for the ideal case. With a total thickness of $3.2 \mu\text{m}$, the R_{on} was calculated to be $0.3 \text{ m}\Omega\text{cm}^2$. Details of the device simulation will appear elsewhere.

III. DEVICE FABRICATION

Fig. 1 shows the schematic cross section of the fabricated device. On (0001)C 4H-SiC n^+ substrates with 8° of inclination toward $\langle 11\bar{2}0 \rangle$, a highly-resistive (HR) layer and the SJ structure with four n-layers and five p-layers were successively grown by chemical vapor deposition in a horizontal cold-wall reactor [12]. The HR layer was designed to isolate the devices from the conducting substrates. The source gases were SiH_4 (0.50 sccm) and C_3H_8 (0.33 sccm), and the carrier gas was H_2 (3 slm). The growth temperature was 1500°C . Under these conditions, the growth rate was about $3.0 \mu\text{m/h}$. The thickness of the HR layer was about $9 \mu\text{m}$. The thickness of each layer in the SJ structure was $0.4 \mu\text{m}$, except for the outermost p-layers for which the thickness was halved to ensure full depletion. The doping concentrations of n-layers in the SJ were designed to be $4 \times 10^{17} \text{ cm}^{-3}$ with N_2 , and those of p-layers were varied in the range of $2.5\text{--}6.5 \times 10^{17} \text{ cm}^{-3}$ with B_2H_6 .

A ring-like mesa structure made of SJ, with the cathode on the interior and the anode on the exterior, was employed, as shown in Fig. 1. The inner and outer diameters of the SJ ring were $165\text{--}170 \mu\text{m}$ and $180\text{--}185 \mu\text{m}$, respectively, at the top of mesa. The SJ length was $10\text{--}20 \mu\text{m}$. Because of a limited vertical depth (about $3 \mu\text{m}$) of ion implantation into the contact regions, sloped sidewalls for the anode and cathode regions were formed on both of the inner and outer sides. To form the slope, molten KOH etching at $460\text{--}480^\circ\text{C}$ using an Al mask [13] was

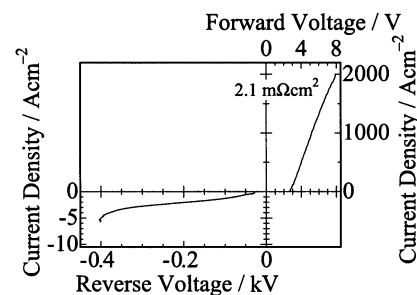


Fig. 2. Typical I - V characteristics of fabricated diodes.

employed to form the mesa with $3\text{--}4 \mu\text{m}$ of height. The anode and cathode regions were formed by Al (average concentration: $1 \times 10^{20} \text{ cm}^{-3}$) and P (average concentration: $2 \times 10^{20} \text{ cm}^{-3}$) ion implantation, respectively, at 300°C . After activation annealing at 1750°C for 30 min in an Ar ambience, the samples were passivated with a thermal oxide grown at 1100°C for 15 min in a dry ambience. As contact metals for the anode and cathode, Al/Ti and Ni, respectively, were thermally evaporated, and they were simultaneously sintered at 800°C for 10 min in an Ar ambience.

IV. ELECTRICAL PROPERTIES OF DIODES

Fig. 2 shows typical current-voltage (I - V) characteristics of the fabricated $p^+/SJ/n^+$ diodes. For forward bias conditions, very high on-state current densities of 100 A/cm^2 at 3.0 V , 500 A/cm^2 at 3.9 V and 1000 A/cm^2 at 5.0 V were obtained. The R_{on} was $2.1 \text{ m}\Omega\text{cm}^2$, where the device active area was defined based on the foot of SJ mesa ring, as schematically indicated by dashed circles in Fig. 1. The obtained R_{on} is about $10\times$ larger than the value (about $0.3 \text{ m}\Omega\text{cm}^2$) predicted by our numerical simulation. The discrepancy between the measured and predicted R_{on} s may be attributed to the high sheet and/or contact resistances in the contact regions, which were not taken into account in the simulation. It should also be noted that our definition overestimates the device active area by 2–3 times, because we included $5\text{--}10 \mu\text{m}$ for each contact region. With microfabrication technologies, the R_{on} should be much reduced.

For reverse bias conditions, the maximum breakdown voltage of 400 V was obtained. This breakdown voltage is more than three times higher than that of conventional (uniformly-doped) p-n diodes with such high doping concentrations ($4 \times 10^{17} \text{ cm}^{-3}$), which should be at most 130 V [11], indicating that the SJ structure operates effectively.

As mentioned before, the breakdown voltage may be reduced by charge imbalance. However, we did not see a systematic change of breakdown voltage when the doping in the p-layers was varied. Therefore, the breakdown voltage was probably reduced by an insufficient device fabrication process: Because of the poor controllability of KOH etching process, the mesas for most of the fabricated diodes were too high and eventually the HR layers were too thin (mostly less than $5 \mu\text{m}$), causing premature breakdown (at less than 650 V even without electric field crowding) in the HR layer. The next step is to develop a reliable and controllable device fabrication process.

V. CONCLUSION

Using epitaxial multiple p-n junction structures of 4H-SiC, lateral SJ diodes were designed, and fabricated for the first time. Owing to relatively high doping concentrations in the SJ region ($4 \times 10^{17} \text{ cm}^{-3}$), very high on-state current densities of 500 A/cm^2 at 3.9 V and 1000 A/cm^2 at 5.0 V were obtained. The breakdown voltage of the device was 400 V, which is more than $3\times$ higher than that of conventional (uniformly-doped) devices (130 V) with such high doping concentrations, indicating the effective operation of SJ structure. These results indicate the prospect of SiC lateral SJ structures, after the device fabrication processes are well established.

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